REMARKS

Claims 1-15 are pending in this application. Claims 1, 9, 13 and 14 are the independent claims. Claim 13 includes a number of means-plus-function clauses which must be given interpretations in accordance with 35 U.S.C. Section 112, ¶6. All claims stand rejected.

Claim 11 is being amended to correct an obvious error, by amending the limitation "the first direction" to "the direction away from the first end" as recited in base Claim 9.

Rejection of Claims 6 and 12 under 35 U.S.C. § 112

Claim 6 and 12 have been rejected under 35 U.S.C. § 112 as being indefinite for failing to particularly point out and distinctly claim the subject matter regarded as the invention. In particular, Claims 6 and 12 recite the limitation "the first edge" without antecedent basis. Accordingly, Claim 6 has been amended to depend from Claim 4, and thus now inherits the respective antecedent basis "a first edge." Claim 12 has been amended to depend from Claim 11 and to recite the "reference clock edges" as recited in Claim 11. As a result, it is believed that the § 112 rejection of Claims 6 and 12 is now overcome, and reconsideration is requested.

Applicant further notes, in response to Examiner's statement on page 2, section 4 of the present Office Action, that "the first edge of the reference clock" refers to an edge of the reference clock, while "the edge of the feedback clock" is an edge of the feedback clock. These limitations are similar in that they relate to clock signals, but different in that the former relates to the reference clock, while the latter relates to the feedback clock. An example of these limitations is illustrated in Fig. 6 of the Specification, where the reference clock CLK_REF has a rising edge at time 502, while the feedback clock has a rising edge at time 504.

Rejection of Claims 1-3, 6 and 9-13 under 35 U.S.C. 102(b)

Claims 1-3, 6 and 9-13 have been rejected under 35 U.S.C. 102(b) as being anticipated by Ishiwaki (U.S. Patent No. 6,407,597). Applicants respectfully disagree with this rejection for the reasons set forth below.

To aid in understanding the present invention, an example embodiment is described below. It will be understood that this embodiment is illustrative and is not intended to limit the scope of the invention being defined by the claims.

A prior art delay-lock loop (DLL) circuit is shown in Figs. 1 and 2. The DLL includes a voltage-controlled delay (VCD) 102 and a phase detector 104. The DLL can also be reset.

After a reset of the DLL, the VCD 102 could, for example, be reset to a minimum delay and the phase relationship between CLK_REF and CLK_FB might, for example, be such that the phase detector issues a "DOWN" command to decrease the VCD delay. In such a situation however, as a result of the VCD being already at a minimum delay, the VCD does not respond to this command. As a result, the DLL cannot achieve a "lock" between the signals.

The example phase detector 412 illustrated in Fig. 4 addresses this problem, utilizing an initialization circuit 410. After a reset at RESETb, either clock signal may be received first. However, the initialization circuit 410 disables the phase detector until the CLK_REF has been received. Further, the "DOWN" command (to decrease the delay) is disabled until the feedback clock CLK_FB has also been received. As a result, the circuit after a reset only allows an increase in delay of the VCD, and allows a decrease in delay only after this increase (Specification, page 8 lines 16-25). The illustrated initialization circuit therefore prevents the DLL from encountering a no-lock condition as described above.

Ishiwaki describes an error correction mechanism for a phase-locked loop (PLL) circuit. As shown in Figs. 1-2, a PLL circuit 8 receives an external clock CLK and generates an internal clock ICLK that has a frequency *n* times that of the external clock CLK (Ishiwaki, col. 4, lines 57-61). To ensure the internal clock ICLK is synchronized with the external clock CLK, the ring counter 10 divides, by *n*, the internal clock ICLK to produce RCLK (col. 5, lines 3-8). A phase comparator 8b then compares the phase of CLK and RCLK, and controls the shift register 8c and delay line 8d to adjust the phase of ICLK (col. 5, lines 16-27). Further, in Fig. 3, the ring counter 10 also has a reset circuit 16 that resets the ring counter 10 in response to detecting an abnormal state in the holding circuits 14 (col 3, lines 47-58 and col. 6, lines 56-59).

Ishiwaki fails to teach the delay locked loop or method as recited in any of Claims 1, 9 and 13. Contrary to Examiner's assertions, Ishiwaki teaches a circuit that is almost entirely

different from the claimed invention. In particular, the ring counter 10 of Ishiwaki does not operate as the claimed initialization circuit, at least for the following reasons:

1) In contrast to the claimed initialization circuit operating "after reset of the delay locked loop," the ring counter 10 merely resets itself upon detecting an error at its holding circuits 14 (col. 6, lines 56-59). Ishiwaki does not suggest resetting the PLL 8; nor does he suggest the ring counter 10 responding to such a reset in any way. It follows, then, that the ring counter 10 cannot "assure[] that the phase detector initially changes the delay..." and "enable[] a change in the delay..." as claimed because these claim limitations refer to a reset of the delay locked loop. Such a reset is not described by Ishiwaki.

2) Ishiwaki provides no suggestion that the ring counter 10 (or any other device) "assures that the phase detector initially changes the delay in a direction away from the first end of the delay range after receipt of one of the reference clock and feedback clock." On the contrary, the ring counter 10 merely performs two unrelated functions: a) it generates a divided-down feedback clock RCLK (col. 4 line 67-col. 5, line 6), and b) it resets itself upon detecting an abnormal state in its hold circuits (col. 6, lines 4-7 and 56-59). The ring counter has no means by which to assure that the phase detector changes delay in any particular direction, because such a change is not controlled by the feedback clock RCLK. Rather, the PLL 8 changes delay according to the comparison of the feedback clock RCLK and external clock CLK, as well as the configuration of the PLL 8. Thus, the ring counter 10 cannot assure a change in delay in a particular direction.

Given (1) and (2) above, it is clear that Ishiwaki does not describe a reset of a delay locked loop; it is the ring counter 10, not the PLL 8, that resets. Yet even if the PLL 8 were to reset, the ring counter 10 has no mechanism by which to "assure" that the PLL 10 changes delay in a particular direction, nor to enable a change in an opposite direction as recited in base Claims 1, 9 and 13. Moreover, Ishiwaki is not concerned with the delay range of the PLL 10, and therefore fails to teach or disclose anything relating to the delay ranges of a PLL, DLL or other feedback device.

Claims 2, 3, 6 and 10-12 depend from one of base Claims 1 and 9 and thus the foregoing applies. As a result, the § 102 rejection of Claims 1-3, 6 and 9-13 cannot stand, and Applicant respectfully requests reconsideration.

Rejection of Claims 4-5, 7-8 and 14-15 under 35 U.S.C. 103(a)

Claims 4-5, 7-8 and 14-15 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshimura et al. (U.S. Patent No. 5,994,934) in view of Ishiwaka.

Examiner states that Yoshimura does not teach "an initialization circuit" as recited in Claim 1 or an "initialization circuit" as recited in Claim 14. However, as explained above, Ishiwaki also fails to teach such an initialization circuit. Claims 4-5, 7-8 and 15 depend from one of base Claims 1 and 14, and therefore inherit the respective "initialization circuit" of the base Claims. Thus, no combination of Yoshimura and Ishiwaki teaches or suggests the delay locked loop, phase detection circuit or method as recited in Claims 4-5, 7-8 and 14-15, and Applicant respectfully requests that the § 102 rejection of these claims be withdrawn.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

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